REMARKS/ARGUMENTS

The Office Action mailed November 24, 2003, has been received and reviewed. Claims 1, 4 through 10, and 13 through 24 are currently pending in the application. Claims 1, 4 through 10, and 13 through 24 stand rejected. All claims are amended herein to replace the term "said" with the term "the", an equivalent term that does not reduce the scope of the claims or surrender any equivalents thereto. No substantive amendments have been made. Reconsideration is respectfully requested.

Information Disclosure Statement(s)

Applicants note the filing of an Information Disclosure Statement herein on June 19, 2003, and note that no copy of the PTO-1449 was returned with the outstanding Office Action. Applicant respectfully requests that the information cited on the PTO-1449 (which is the same as that of record to that date in the parent application hereto) be made of record herein.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 6,274,423 to Prall et al. in view of U.S. Patent No. 6,124,626 to Sandhu et al., and U.S. Patent No. 6,399,982 to Derderian et al.

Claims 1, 4, 6 through 10, 13 through 15, and 17 through 24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Prall et al. (U.S. Patent No. 6,274,423) in view of Sandhu et al. (U.S. Patent No. 6,124,626), and Derderian et al. (U.S. Patent No. 6,399,982). Applicants respectfully traverse this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

Prall discloses an etch process for aligning a capacitor and an adjacent contact corridor. Applicants respectfully submit that the Derderian and Sandhu references are disqualified as prior art against the claimed invention because the subject matter and the claimed invention "were, at the time the invention was made, owned by the same person or subject to an assignment to the same person." *See, MPEP* §706.02(l)(1); 35 U.S.C.§103(a). Neither reference has a publication date prior to the filing date of the predecessor application (U.S. 09/399,592 filed September 20, 1999) from which the present case claims priority. For Example, Sandhu issued September 26, 2000 (and its parent case application no. 08/918,634 issued March 13, 2001). Derderian issued June 4, 2002 (and its parent case, application no. 08/887,915 issued February 13, 2001).

In the Statement of Common Ownership filed herewith, it is submitted that U.S. Patent No. 6,399,982 to Derderian et al., U.S. Patent No. 6,124,626 to Sandhu et al. and the present application were, at the time the invention was made, owner by, or subject to an obligation of assignment to the same entity, namely Micron Technology, Inc. Applicants respectfully submit that such a statement is sufficient evidence to establish common ownership and to disqualify U.S. Patent No. 6,399,982 to Derderian et al. and U.S. Patent No. 6,124,626 to Sandhu et al. from being used as prior art against the claims of the above-entitled application. *MPEP* § 1706.02(l)(2)II. Reconsideration and withdrawal of the rejections in view of U.S. Patent No. 6,399,982 to Derderian et al. and U.S. Patent No. 6,124,626 to Sanhu et al. is respectfully requested.

By way of contrast with Prall, claim 1 of the presently claimed invention recites a "DRAM circuit comprising: a substrate having an active region thereon and a capacitor structure disposed above the active region, the capacitor structure including a storage node, a dielectric layer overlying the storage node, and a conductive cell plate overlying the dielectric layer, each of the dielectric layer and the conductive cell plate having an end portion proximate a conductive contact, the conductive contact extending downward and adjacently beside the capacitor structure, the end portion of the dielectric layer extending closer to the conductive contact than the end portion of the conductive cell plate; a first TEOS layer disposed proximate the storage node; a second TEOS layer disposed over the capacitor structure and encasing the end portions of the dielectric layer and the conductive cell plate, the second TEOS layer disposed between the

capacitor structure and the conductive contact; and a doped BPSG layer disposed over the second TEOS layer, the conductive contact extending through the BPSG layer and the second TEOS layer."

Applicants respectfully submit that Prall fails to teach or suggest every element of claim 1 of the presently claimed invention. Specifically, Prall fails to teach or suggest a first TEOS layer disposed proximate the storage node and a second TEOS layer over the capacitor structure and encasing the end portions of the dielectric layer and the conductive cell plate, the second TEOS layer disposed between the capacitor structure and the conductive contact. As Prall fails to teach or suggest every element of the presently claimed invention, applicants submit that independent claim 1 is not rendered obvious by Prall. Thus, claim 1 is allowable.

Claims 4 through 9, 21 and 22 are each allowable as depending, either directly or indirectly, from allowable claim 1.

Claim 9 is further allowable as Prall fails to teach or suggest that the TEOS layer is a dopant barrier between the capacitor structure and the BPSG layer.

Claim 21 is further allowable as Prall fails to teach or suggest the first TEOS layer is configured to prevent diffusion of contaminants into the active region.

Claim 22 is further allowable as Prall fails to teach or suggest the first TEOS layer comprises a thickness of about 100 Å to about 250 Å.

Independent claim 10 of the presently claimed invention is allowable at least for the same reasons as independent claim 1 of the presently claimed invention. By way of contrast with Prall, claim 10 of the presently claimed invention recites a "semiconductor memory device comprising: a semiconductor substrate having an active region thereon and a capacitor structure formed above the active region, the capacitor structure including a first conductive layer, a second conductive layer, and a dielectric layer, the dielectric layer disposed between the first and second conductive layers, each of the dielectric layer and the first and second conductive layers having an end portion proximate a conductive contact, the conductive contact extending downward and adjacently beside the capacitor structure, the end portion of the dielectric layer extending closer to the conductive contact than the end portion of each of the first conductive layer and the second conductive layer; a diffusion barrier proximate the first conducting layer and configured to

prevent diffusion of contaminants into the active region; a TEOS layer disposed over the capacitor structure and encasing the end portions of the dielectric layer and each of the first conductive layer and the second conductive layer, the TEOS layer disposed between the capacitor structure and the conductive contact; and a doped BPSG layer disposed over the TEOS layer, the conductive contact extending through the BPSG layer and the TEOS layer."

Applicants respectfully submit that Prall fails to teach or suggest every element of the presently claimed invention. Specifically, Prall fails to teach or suggest "a diffusion barrier proximate the first conducting layer and configured to prevent diffusion of contaminants into the active region" or "a TEOS layer disposed over the capacitor structure and encasing the end portions of the dielectric layer and each of the first conductive layer and the second conductive layer, the TEOS layer disposed between the capacitor structure and the conductive contact; and a doped BPSG layer disposed over the TEOS layer, the conductive contact extending through the BPSG layer and the TEOS layer."

Prall fails to teach or suggest a diffusion barrier proximate a first conducting layer and configured to prevent diffusion of contaminants into an active region. Further, Prall lacks fails to teach or suggest a TEOS layer, a BPSG layer disposed over the TEOS layer or a conductive contact extending through a doped BPSG layer and TEOS layer. As Prall fails to teach or suggest every element of the presently claimed invention, applicants submit that independent claim 10 is not rendered obvious by Prall. Thus, claim 10 is allowable.

Claims 13 through 20 are each allowable as depending, either directly or indirectly, from allowable claim 10.

Claim 20 is further allowable as Prall fails to teach or suggest that the TEOS layer is a dopant barrier between the capacitor structure and the BPSG layer.

Claim 23 is further allowable as Prall fails to teach or suggest a diffusion barrier comprising a nitride layer or TEOS layer.

Claim 24 is further allowable as Prall fails to teach or suggest a diffusion barrier comprising a thickness of about 100 Å to about 250 Å.

Obviousness Rejection Based on U.S. Patent No. 6,274,423 to Prall et al., U.S. Patent No. 6,124,626 to Sandhu et al, and U.S. Patent No. 6,399,982 to Derderian et al., and further in view of U.S. Patent No. 5,763,306 to Tsai

Claims 5 and 16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Prall et al. (U.S. Patent No. 6,274,423), Sandhu et al. (U.S. Patent No. 6,124,626), and Derderian et al. (U.S. Patent No. 6,399,982), and further in view of Tsai (U.S. Patent No. 5,763,306). Applicants respectfully traverse this rejection, as hereinafter set forth.

Applicants respectfully submit that Derderian and Sandhu are not appropriate prior art references under 35 U.S.C. §103(a). Further, the Court of Appeals for the Federal Circuit has stated that "dependent claims are nonobvious under section 103 if the independent claims from which they depend are nonobvious." In re Fine, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988). See also MPEP § 2143.03. Having failed to teach or suggest each and every limitation of the current application, the prior art referenced as rendering dependent claims 5 and 16 obvious, cannot serve as a basis for rejection.

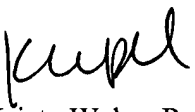
ENTRY OF AMENDMENTS

The amendments to the claims above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application.

CONCLUSION

Claims 1, 4 through 10, and 13 through 24 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Office determine that additional issues remain which might be resolved by a telephone conference, the Examiner is respectfully invited to contact Applicants' undersigned attorney.

Respectfully submitted,



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